REMARKS

Claims 1, 3-12, 14-18, 20-22 and 24-38 were pending prior to this paper.

In this paper, the Applicant has amended the claims by replacing all occurrences of the term "cell(s)" with the term "packet(s)". The Applicant submits that this amendment is supported by the specification as originally filed (see, for example, paragraph [0029]) and does not narrow the scope of the claims. The Applicant has made additional amendments to claims 1, 3, 4, 8, 12 and 33-38. The amendments to claims 1, 3, 4, 8, 12 and 33-38 are also submitted to be supported by the application as originally filed and to add no new matter.

Allowed Subject Matter

Claims 11 and 18 stand allowed. The Applicant submits that claims 11 and 18, as amended to replace the term "cell(s)" with the term --packet(s)--, are also allowable over the prior art of record.

Formal Objections

The Applicant has amended claims 3, 4 and 33-38 to replace the phrase "An apparatus according to" with --The apparatus of--, as suggested by the Examiner. It is submitted that these amendments obviate the Examiner's formal objections to claims 3, 4 and 33-38.

Objections Based on Prior Art

The Examiner has raised the combination of U.S. Patent No. 6,775,305 (Delvaux) and PCT Publication No. WO 96/17489 (Vallée et al) in connection with claims 1, 3-10, 12, 14-17, 20-22 and 24-38.

The Applicant submits that claims 1, 3-10, 12, 14-17, 20-22 and 24-38 patentably distinguish the combination of Delvaux and Vallée et al. and requests reconsideration of these claims in light of the following submissions.

Claims 1, 3-5 and 33-38

The Applicant submits that claims 1, 3-5 and 33-38 patentably distinguish the combination of Delvaux and Vallée et al.

The Office Action expresses the view that Delvaux discloses a number of the claim 1 features including "a first demultiplexer for dividing data [cells/packets] of a high-rate data stream into N sub-streams, so that each sub-stream carries every N^{th} data [cell/packet] of the high-rate data stream and data [cells/packets] in the N sub-streams are staggered in time with respect to one another". The Applicant submits this aspect of Delvaux is misinterpreted in the Office Action.

As understood, Delvaux discloses a multi-channel communication link 140 that connects an edge ATM switch 12*b* with a computing device 15*d* - see Figure 8. The Delvaux system inserts a sequence number into each individual ATM cell at an interface 115 between ATM switch 12*b* and a corresponding physical layer FIFO 142*a* - see col. 16, ln. 37-41. The sequence number is necessary in the Delvaux system to reassemble the cells in the correct sequence after they have been transmitted across communication lines 146. Delvaux refers to the combination of the ATM cell and the sequence number as a transport protocol data unit (TPDU) - see col. 16, ln. 52-56. Delvaux discloses that the streams of TPDUs are inverse-multiplexed for transmission across available physical communication lines 146. TPDUs are transferred at a greater frequency to the lines 146 capable of supporting a higher bit transfer rate -see col. 16, ln. 64 - col. 17, ln. 8. Delvaux discloses that TPDUs may be simultaneously transferred on different communication lines 146 - see col. 17, ln. 9-20 which describes an example wherein a first TPDU is sent on line 146_0 and a second TPDU is sent simultaneously on line 146_1.

In contrast to the Delvaux system, claim 1 recites "a first demultiplexer for dividing data packets of a high-rate data stream into *N* sub-streams, so that each sub-stream carries every N^{th} data packet of the high-rate data stream and data packets in the *N* sub-streams are staggered in time with respect to one another".

Delvaux fails to disclose or suggest these claim 1 features. In Figure 9, Devlaux shows a transmit timing diagram for a system having two communication lines (referred to as "line 0" and "line 1"). Figure 9 shows that the first, second and third TPDUs (references 163_0, 163_1, and 163_2) are sent on line 1 and that the fourth and seventh TPDUs (references 163_3 and 163_6) are sent on line 0. This aspect of Delvaux is also described at col. 18, ln. 56 - col. 19, ln. 1. Figure 9 shows that line 1 has a higher bit transfer rate than line 0 and therefore a disproportionately larger number of TPDUs are sent on line 1. Moreover, Figure 9 shows that immediately successive TPDUs are sent on line 1. Accordingly, Delvaux fails to teach or suggest "each substream carries every N^{th} data packet" as recited in claim 1. In Delvaux, higher-capacity communication lines carry more TPDUs than other communication lines.

Further, Figure 9 clearly shows that the cells identified by references 163_2 and 163_3 are transmitted during overlapping time slots. This aspect of the Delvaux system is described at col. 17, ln. 9-20 which provides an example wherein a first TPDU is sent on line 146_0 and a second TPDU is sent "simultaneously" on line 146_1. Delvaux therefore fails to disclose the claim 1 feature that the data packets in the *N* sub-streams are "staggered in time with respect to one another".

The Office Action also expresses the view that Delvaux discloses the claim 1 combination of "[d]ata transmission apparatus for ... delivering the high-rate data streams over a mid-plane having a limited number of signal conductors" and "a plurality of data transmitting devices, each data transmitting device ... transmitting the serialized data via a corresponding first serial data connection over said mid-plane to a data receive interface" [Emphasis Added]. The Applicant submits that this is not an accurate characterization of Delvaux.

Delvaux describes a multi-channel communication link 140 that connects an edge ATM switch 12*b* with a computing device 15*d* -see col. 16, ln. 8-12 which the multi-channel link 140 (Figure 8) is meant to replace link 11 (Figure 1) between ATM switch 12*b* and computing device 15*d*. Delvaux does not disclose serialized data transmission between a data transmitting device and a data receive interface over a pin-limited mid-plane as recited in claim 1.

Vallée et al. fail to remedy these deficiencies.

Given the foregoing differences, the Applicant submits that claim 1 patentably distinguishes the combination of Delvaux and Vallée et al. Claims 3-5 and 33-38 depend from claim 1 and are submitted to be patentable over Delvaux and Vallée et al. for at least this reason.

Claims 6 and 7

The Applicant submits that claims 6 and 7 patentably distinguish the combination of Delvaux and Vallée et al.

The Office Action expresses the view that Delvaux discloses a number of claim 6 features including "a first demultiplexer connected to receive the data stream and to split the data stream by delivering the transmit [cells/packets] in rotation into a plurality of N transmit channels, so that each said transmit channel carries every N^{th} transmit [cell/packet]". As submitted above, Delvaux does not disclose that each of N transmit channels carries every N^{th} transmit packet as recited in claim 6. Delvaux teaches away from this aspect of claim 6 by describing how successive TPDUs can be sent on the same line and how lines having relatively high transmit rates can be assigned a relatively large number of TPDUs for transmission - see Figure 9.

The Office Action also expresses the view that Delvaux discloses "a plurality of data transmitting devices, each data transmitting device connected ... to output the transmit [cells/packets] of the corresponding one of the N transmit channels on a corresponding data

connection for transmitting data over a mid-plane to the receiver, wherein each data transmitting device comprises a serializer device and the corresponding data connection comprises a serial data connection". As submitted above, Delvaux fails to disclose or suggest transmission of serialized data between a data transmitting device and a receiver over a mid-plane as recited in claim 6.

In addition, the Office Action contends that Delvaux discloses the claim 6 feature of "first receive control circuit configured to determine a sequence of arrival of the receive [cells/packets] in the plurality of buffers and to place the receive [cells/packets] onto a bus in the sequence of arrival". The Applicant submits that Delvaux does not determine "a sequence of arrival of the receive packets" or place receive packets onto a bus "in the sequence of arrival" as recited in claim 6. The sequence of arrival has no relevance in Delvaux because the correct ordering of the TPDUs can be ascertained from the sequence numbers. Delvaux teaches that sequence numbers—which are inserted into each of the TPDUs prior to transmission—are used to reassemble the TPDUs into the correct order at the receiving end. Some TPDUs arrive out of sequence as shown in Figure 10 and described at col. 19, ln. 16-54. For example, Figure 10 clearly shows TPDU 173_3 arriving at MUX/DEMUX 144*b* prior to TPDU 173_1, even though TPDU 173_1 is placed in output FIFO 142*b* at a location that precedes TPDU 173_3. Delvaux teaches further at col. 17, ln. 28-34, that a "resequencing buffer" is used at the receiving end to rearrange TPDUs into sequence number order and that TPDUs are held in the resequencing buffer "until all TPDUs preceding the present TPDU have been received and released". Thus, in the Delvaux system, TPDUs are received out of order. Accordingly, the Delvaux system does not reassemble TPDUs onto a bus in accordance with their "sequence of arrival" as recited in claim 6.

Vallée et al. fail to remedy these deficiencies.

As correctly identified by the Examiner (at p. 7 of the Office Action), Delvaux does not disclose the claim 6 combination of "a first transmit control circuit connected to the data transmitting devices, the first transmit control circuit configured to cause the data transmitting devices to output the transmit [cells/packets] in sequence with commencement of transmission

of the transmit [cells/packets] from sequential data transmitting devices staggered in time relative to one another by a time difference ΔT" and "wherein the first receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q [cells/packets], with $Q \geq 1$ and wherein the first transmit control circuit is configured to transmit the flow control signal with the transmit [cells/packets] to the receiver".

The Office Action expresses the view that Vallée et al. disclose these claim 6 features. The Applicant submits that this is not correct.

As understood, Vallée et al. disclose a method of inverse-multiplexing a series of ATM cells and sending the ATM cells between ATM switches (ATM Inverse Multiplexers) over a plurality of transmission links - see Figures 4 and 8. Each ATM data cell is assigned a sequence number. However, sequence number information is only carried in separate SN cells, which are transmitted across the available links prior to transmitting ATM data cells - see p. 8, ln. 26-32 and p. 9, ln. 21-22. The receiving node uses the SN cells to determine the sequence in which to read the subsequently transmitted ATM data cells as well as the differential delay among individual links - see p. 8, ln. 31-35.

The Office Action specifically cites p. 8, ln. 26-35 of Vallée et al. as disclosing the claim 6 feature of a first transmit control circuit "configured to cause the data transmitting devices to output the transmit [cells/packets] in sequence with commencement of transmission of the transmit [cells/packets] from sequential data transmitting devices staggered in time relative to one another by a time difference ΔT". This passage of Vallée et al. describes sending SN cells which carry sequence number information back and forth between AIMs so that the receiving AIM can retrieve "the original cell sequence" and "the differential delay among individual links". No part of this cited passage discloses or suggests staggering the commencement of transmission of SN cells or ATM data cells over the available links by a constant "time difference ΔT", as claimed.

In contrast, Vallée et al. specifically disclose that "bursts" of SN cells are sent out across all the links (p. 9, ln. 21-30 and p. 10, ln. 35-37) to determine the delays among links.

This suggests that groups of cells are transmitted over the multiple transmission links concurrently, rather than being "staggered" across the links relative to one another by a constant "time difference ΔT". Moreover, if there is a delay detected by the Vallée et al. receiving end, such delay is due to the differential delay among individual links. Such delay is a characteristic of each link. Vallée et al. do not suggest that such delay is attributable to a control circuit staggering commencement of packet transmission over the links. Vallée et al. therefore do not disclose or suggest a transmit control circuit which causes commencement of transmission of transmit packets to be "staggered in time relative to one another by a time difference ΔT" as recited by claim 6.

The Office Action specifically cites p. 6, ln. 26-35 of Vallée et al. as disclosing the claim 6 feature of "wherein the first receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q [cells/packets], with $Q \geq 1$ and wherein the first transmit control circuit is configured to transmit the flow control signal with the transmit [cells/packets] to the receiver". This passage of Vallée et al. describes how SN cells are sent from the receiving end of the Vallée et al. system back to the transmitting node. No part of this cited passage describes a buffer at the receive end or a receive control circuit configured to issue a flow control signal when such a buffer "has a remaining capacity of Q packets, with $Q \geq 1$" as recited in claim 6.

In contrast, Vallée et al. disclose that SN cells (originating from the transmitting node) are queued at the receiving end until the receiving end determines the sequence in which to read the ATM data cells from the incoming links - see p. 8, ln. 33-35. The receiving end then starts sending SN cells of its own, with an AIMFERR code set to indicate that it is ready to receive data cells. The transmitting node waits until it receives these SN cells with the AIMFERR code from the receiving end, before proceeding to send ATM data cells - see p. 8, ln. 32 - p. 9, ln. 4. There is no suggestion by Vallée et al. that a signal will be sent by the receiving end to notify the transmitting node that a receive buffer has reached a certain remaining capacity. Signals are only sent by the receiving end to indicate that the SN cell sequence has been determined and that a particular link is ready to receive ATM data cells. Therefore, Vallée does not teach a first receive control circuit "configured to issue a flow

control signal when any one of the buffers has a remaining capacity of Q packets, with $Q \geq 1$" as recited in claim 6.

In view of the foregoing distinctions, the Applicant submits that claim 6 patentably distinguishes the combination of Delvaux and Vallée et al. Claim 7 depends from claim 6 and is submitted to be patentable over Delvaux and Vallée et al. for at least this reason.

Claims 8-10

The Applicant submits that claims 8-10 patentably distinguish the combination of Delvaux and Vallée et al.

The Office Action expresses the view that Delvaux discloses a number of the claim 8 features, including "a first demultiplexer connected to receive the data stream and to split the data stream by delivering the transmit [cells/packets]in rotation into a plurality of ***N*** transmit channels, so that each said transmit channel carries every N^{th} transmit [cell/packet]". As submitted above, Delvaux does not disclose or suggest that each of ***N*** transmit channels carries every N^{th} transmit packet as recited in claim 8.

Vallée et al. fail to remedy this deficiency.

The Examiner correctly identifies (at pp. 9-10 of the Office Action) that Delvaux does not disclose the claim 8 combination of "a first transmit control circuit configured to cause the data transmitting devices to output the transmit [cells/packets] in sequence with commencement of transmission of the transmit [cells/packets] from sequential data transmitting devices staggered in time relative to one another by a time difference ΔT". The Office Action expresses the view that Vallée et al. disclose this feature. The Applicant submits that this is not correct. As submitted above, Vallée et al. fail to teach or suggest staggering the commencement of transmission of transmit packets from sequential data transmitting devices "relative to one another by a time difference ΔT".

Claim 8 (as amended) also recites "wherein: the first transmit interface is located on a line card of a network element having an interface for receiving the data stream, the receiver is located on a second card of the network element, and the serial data connections comprise data lines extending between the line card and the second card through a mid-plane of the network element". That is, the claim 8 "first transmit interface" and the claim 8 "receiver" are located on the same network element and transmission between the transmit interface and the receiver takes place through "a mid-plane of the network element". Neither Delvaux nor Vallée et al. disclose this claim 8 feature. In contrast, Delvaux describes a multi-channel communication link 140 that connects an edge ATM switch 12*b* with a computing device 15*d*. Vallée et al. describe a system for communication between ATM network elements (see the ATM switches of Figure 2 and AIMs of Figures 4 and 8) and not for communication within a particular network element as recited in claim 8.

Based on this reasoning, the Applicant submits that claim 8 patentably distinguishes the combination of Delvaux and Vallée et al. Claims 9 and 10 depend from claim 8 and are submitted to be patentable over Delvaux and Vallée et al. for at least this reason.

Claims 12 and 14-17

The Applicant submits that claims 12 and 14-17 patentably distinguish the combination of Delvaux and Vallée et al.

The Office Action expresses the view that Delvaux discloses a number of the claim 12 features, including the combination of "means for carrying a data stream comprising a sequence of [cells/packets] having an order;" and "means for receiving the [cells/packets] in the order at the receiver." As explained above, Delvaux fails to teach or suggest that packets are received in order as recited in claim 12. In contrast, Delvaux teaches that sequence numbers—which are inserted into each of the TPDUs prior to transmission—are used to reassemble the TPDUs into the correct order in a resequencing buffer at the receiving end, even though the TPDUs are received out of order. Figure 10 and col. 19, ln. 16-54 explicitly show how the Delvaux TPDUs are received out of order at MUX/DEMUX 144*b*. For

example, Figure 10 shows that TPDU 173_3 arrives at MUX/DEMUX 144*b* prior to TPDU 173_1, even though the cell corresponding to TPDU 173_1 precedes the cell corresponding to TPDU 173_3 in input FIFO 142*a*. Accordingly, the Delvaux system does not teach or suggest the combination of "a data stream comprising a sequence of packets having an order" and means for receiving "packets in the order at the receiver" as recited in claim 12.

The Office Action also expresses the view that Delvaux discloses the claim 12 feature of "transmitting means for transmitting the packets in each channel to a receiver by way of signal conductors in a mid-plane." As submitted above, Delvaux does not teach or suggest transmission of packets over a mid-plane.

Vallée et al. fail to remedy these deficiencies.

The Examiner correctly identifies (at p. 12 of the Office Action) that Delvaux fails to disclose the claim 12 feature of "control means for commencing the transmission of individual packets to the receiver, in the order, at times staggered relative to one another by a time difference ΔT that exceeds a worst case inter-channel difference in latency for transmission of packets from the transmitting means to the receiver by way of the mid-plane". The Examiner expresses the view that Vallée et al. disclose this feature. The Applicant submits that the Examiner has misinterpreted this aspect of Vallée et al. As submitted above, Vallée et al. do not teach or suggest "commencing the transmission of individual packets" at times "staggered relative to one another by a time difference ΔT" as recited in claim 12.

Claim 12 recites further that the temporal staggering interval ΔT "exceeds a worst case inter-channel difference in latency for transmission of packets". Vallée et al. do not disclose or suggest this claim 12 feature. The Vallée et al. system makes use of sequence number cells (SN cells) to recover the order of ATM data cells transmitted over the links. The Vallée et al. has no need or desire to wait for a time interval ΔT that "exceeds a worst case inter-channel difference in latency for transmission of packets". Such waiting may needlessly slow down the Vallée et al. communication system.

Based on this reasoning, the Applicant submits that claim 12 patentably distinguishes the combination of Delvaux and Vallée et al. Claims 14-17 depend from claim 12 and are submitted to be patentable over the combination of Delvaux and Vallée et al. for at least this reason.

Claims 20-22 and 24-29

The Applicant submits that claims 20-22 and 24-29 patentably distinguish the combination of Delvaux and Vallée et al.

The Examiner correctly identifies (at p. 14 of the Office Action), that Delvaux does not disclose the claim 24 features of "simultaneously transmitting data on each of the channels from the transmitter to the receiver while staggering commencement of transmission of the [cells/packets] assigned to each channel in time relative to one another by a time difference ΔT". The Office Action expresses the view that Vallée et al. disclose this claim 24 feature. The Applicant respectfully submits that this is not correct. As submitted above, Vallée et al. fail to teach or suggest temporally "staggering commencement of transmission of the packets assigned to each channel in time relative to one another by a time difference ΔT".

The Examiner correctly identifies (on pp. 15 and 16) that Delvaux does not disclose the claim 24 feature of "inhibiting transmission of [cells/packets] in at least one of the channels in response to receiving, at the transmitter, a first flow control signal issued from the receiver; and, upon inhibiting transmission of [cells/packets] in the at least one of the channels: waiting without transmission of [cells/packets] in the at least one of the channels; and after waiting, recommencing transmission of [cells/packets] in the at least one of the channels an integer multiple of the time difference ΔT after a time at which transmission of a previous [cell/packet] commenced on the at least one of the channels".

The Office Action expresses the view that Vallée et al. disclose this claim 24 feature. The Applicant submits that this is not correct. The Office Action cites p. 9, ln. 11-15 as disclosing this claim 24 feature. This cited portion of Vallée et al. describes how a transmitting

node waits for SN cells sent from the receiving end to indicate that a particular link is "ready". If the transmitting node receives a SN signal from the receiving end that a particular link is "ready", then the ATM data is sent from the transmitting node to the receiving node on the link. This procedure is performed at initialization (i.e. prior to transmission of ATM data cells) and is repeated until "at least one available link is declared ready". To the extent that such SN cells may be considered "flow control signals", such SN cells do not cause the transmitting node to inhibit transmission of ATM data cells. In contrast, such AIM SN cells (transmitted from the receiving end to the transmitting node of the Vallée et al. system) only indicate that ATM data cells should be sent on a particular link. In fact, the absence of such a SN cell causes the Vallée et al. transmitting node to refrain from transmitting data cells on a particular link.

Claim 24 recites "inhibiting transmission of packets in at least one of the channels in response to receiving, at the transmitter, a first flow control signal issued from the receiver". The Vallée et al. system does not inhibit transmission "in response to receiving" a flow control signal as recited in claim 24. The Vallée et al. actually enables transmission in response to receiving a SN signal from the receiving end.

Claim 24 recites further "after waiting, recommencing transmission of packets in the at least one of the channels an integer multiple of the time difference ΔT after a time at which transmission of a previous packet commenced on the at least one of the channels". The phrase "recommencing transmission of packets" in claim 24 implies that data packets were previously being transmitted over the "at least one of the channels" prior to "recommencing transmission". This contrasts with Vallée et al., which describes refraining from using a particular link at all for the transmission of ATM data cells, unless a SN cell is received from the receiving end to indicate that a particular link is "ready". Vallée et al. do not disclose or suggest commencing transmission of ATM data cells, then inhibiting transmission of ATM data cells and then "recommencing transmission of packets" as recited in claim 24.

Moreover, claim 24 recites "recommencing transmission of packets in the at least one of the channels an integer multiple of the time difference ΔT after a time at which transmission

of a previous packet commenced on the at least one of the channels". Vallée et al. do not teach or suggest anything resembling recommencing transmission of packets after a temporal period that is "an integer multiple of the time difference ΔT after a time at which transmission of a previous packet commenced on the at least one of the channels" as recited in claim 24.

Based on this reasoning, the Applicant submits that claim 24 patentably distinguishes the combination of Delvaux and Vallée et al. Claims 20-22 an 25-29 depend from claim 24 and are submitted to patentably distinguish Delvaux and Vallée et al. for at least this reason.

Claims 30-32

The Applicant submits that claims 30-32 patentably distinguish the combination of Delvaux and Vallée et al.

The Office Action expresses the view that Delvaux discloses a number of the features of claim 30 including "[a] method for transmitting a sequence of [cells/packets], in order ..." and "in each of the channels, transmitting the [cells/packets] in the sequence in order of the sequence from the transmitting device to the receiving device over one or more serial data connections". As submitted above, Delvaux does not disclose transmitting TPDUs in sequential order. This can be seen from Figure 9 of Delvaux, which clearly shows that TPDU 163_6 is transmitted prior to TPDU 163_5, even though the cell corresponding to TPDU 163_5 precedes the cell corresponding to TPDU 163_6 in the sequence of input FIFO 142*a*.

The Examiner expresses the view that Delvaux discloses the claim 30 feature of "receiving transmitted [cells/packets] at the receiving device in the same order that the transmitted [cells/packets] were transmitted from the transmitting device". As discussed above, claim 30 recites that cells are transmitted in the order of their sequence. As clearly shown in Figure 9, Delvaux describes transmitting TPDU 163_1 on line 1 prior to transmitting TPDU 163_3 on line 0, while Figure 10 shows TPDU 173_3 arriving at the receiving end (MUX/DEMUX 144*b*) prior to TPDU 173_1. Accordingly, Delvaux teaches that TPDUs are received in a different order than they are transmitted. Delvaux does not rely on transmitting

or receiving TPDUs in order, as the Delvaux system makes use of sequence numbers which allow reassembly of TPDUs even where the TPDUs are received out of order.

Vallée et al. fail to remedy these deficiencies.

The Examiner correctly identifies that Delvaux does not disclose the claim 30 feature of "the [cell/packet] transmit times for successive channels staggered relative to one another by amounts exceeding any inter-channel differences in skew and latency".

The Office Action contends that Vallée et al. disclose this feature. The Applicant submits that this is not correct. The Office Action cites p. 8, ln, 26-35 of Vallée et al. as disclosing the claim 30 feature of "the [cell/packet] transmit times for successive channels staggered relative to one another by amounts exceeding any inter-channel differences in skew and latency". This passage of Vallée et al. describes the use of SN cells transmitted from the transmitting node to the receiving end and from the receiving end to the transmitting node to allow the receiving end to determine "the sequence in which to read the ATM data cells from the incoming links as well as the differential delay among individual links" and to allow the transmitting node to determine which links are "ready" to transmit ATM data cells. No part of this passage, nor any other aspect of Vallée et al., makes any suggestion of staggering cell transmit times for successive channels by "amounts exceeding any inter-channel differences in skew and latency" as recited in claim 30. The Vallée et al. system has no need for such staggering, as the exchange of SN cells between the transmitting node and the receiving node allows the receiving node to know the inter-channel sequence and relative delay, which can be used to recover the order of the packets of the transmitted data. Waiting for such periods would needlessly slow down the Vallée et al. communication system.

Based on this reasoning, the Applicant submits that claim 30 patentbaly distinguishes the combination of Delvaux and Vallée et al. Claims 31 and 32 depend from claim 30 and are submitted to patentably distinguish Delvaux and Vallée et al. for at least this reason.

Conclusion

In view of the arguments presented above, the Applicant submits that this application is in condition for allowance and respectfully requests reconsideration and allowance of this application.

Respectfully submitted,

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